



OL_H264LD-CFS
HDTV H.264/AVC Limited
Baseline Video Decoder
With Compressed Frame Store
Rev 0.8

General Description

The OL_H264LD-CFS core is a hardware implementation of the H.264 baseline video compression algorithm. The core decodes a bitstream produced by the OLH264E-CFS encoder and produces a video stream up to the highest HDTV resolution. Simple, fully synchronous design with low gate count.

Applications

- ◆ Digital video recorders.
- ◆ Video wireless devices.
- ◆ Video surveillance systems.
- ◆ Hand held HDTV video cameras.

Features

- ◆ Fully compatible with the output of the OL_H264E-CFS encoder core.
- ◆ Highly (10-15:1) compressed frame store (CFS) with perfect reconstruction (no error/drift) with third party standard decoders. Patent pending technology.
- ◆ Extremely low power : no external DRAM required and much lower bandwidth and power through the CFS.
- ◆ I and P frame support.
- ◆ Supports up to the highest HDTV video resolution (1920x1080 @ 30 fps progressive).
- ◆ Up to Profile level 4.1 can be decoded.
- ◆ Very low operational frequency : from ~1.5 MHz for QCIF @ 15 fps to ~250 MHz for 1920x1080 @ 30 fps.
- ◆ Single core HDTV support in FPGA : 720p (1280x720) at 30 fps in high end FPGAs (Virtex4) . 4 CIF (704x576) at 30 fps in low end FPGAs.
- ◆ No CPU required for decoding.
- ◆ Very low latency decoding
- ◆ Motion vector up to -16.00/+15.75 pixels around the predicted motion vector (-24.00/+23.75 around the origin), down to quarter pixel.
- ◆ Support for most of intra4x4 and all intra16x16 modes.
- ◆ Block skipping logic for lower bitrate.
- ◆ Supports YUV 4:2:0 video output.
- ◆ Min Clock speed = ~4 x the raw pixel clock speed.
- ◆ Simple, fully synchronous design.
- ◆ Available as fully functional and synthesizable VHDL or Verilog soft-core.

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Functional Description

The OL_H264LD-CFS core is a hardware implementation of the H.264 baseline video compression algorithm designed to decode a bitstream created by the OL_H264e core and output progressive video up to HDTV 1920x1080 at 30 fps.

Each block of 16x16 pixels is processed in just 1024 cycles. This means that each pixel is processed in just 4 cycles. Consequently, given an target video stream of resolution X by Y, and frame rate fps, the minimum clock frequency to decode a such bitstream is:

$$F = 4 * X * Y * fps$$

This allows the core to process the video stream at relatively low clock frequencies. For example, HDTV video of 1920x1080 @ 30 fps requires ~250 MHz, whereas VGA video of 640x480 @ 30 fps requires ~37 MHz.

The table below summarizes the relationship between some possible video resolutions and frame rates and the clock frequency of the core.

Resolution	QCIF @ 15 fps	CIF @ 30fps	VGA @ 30fps	1280x720 @ 30fps	1920x1080 @ 30fps
Core freq.	~1.5 MHz	~12.1 MHz	~36.8 MHz	~110.5 MHz	~250.6 MHz

Table 1 Core frequency versus video resolution and frame rate.

Advantages of the core

Some of the key advantages of the core are discussed further below:

Compressed Frame Store (CFS)

The core stores reference images used during motion estimation in a compressed frame store (CFS) using patent pending technology. Depending on the quality required in the H.264 encoded bitstream, compression in the CFS can be as high as 10-15:1. No reconstruction error or drift is present when the output H.264 bitstream is decoded with a third party, standard, decoder.

The table below details the approximate uncompressed reference frame storage requirement for various video resolutions, compared to that required for CFS with an average of ~250 bits/macroblock. This is a 24:1 reduction in external memory compared to the OL_H264E core that requires two full frames of 4:2:0 video.

Resolution	VGA 640x480	D1 720x480	720p 1280x720	1080p 1920x1080
Uncompressed size	450	506.25	1350	3060
Compressed size	~38.4	~43.2	~115.5	~261.2

Table 2 Frame store size comparison, figures in Kbytes (1024 bytes)

The above is only an example and a smaller CFS is possible with lower and still perfectly acceptable quality.

Such low amounts of memory required, even for HDTV, allows direct integration of the CFS memory in a SoC as a single port SRAM, without the need for expensive and power hungry DRAM.

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Extreme Low Power

The CFS brings the additional advantage of extreme low power:

- No expensive and power hungry DRAM required
- No power hungry, fast interface to the external DRAM on the printed circuit board
- Because the data in the CFS is highly compressed, the access to the external memory is sporadic. This means much lower bandwidth and, hence, power.

HDTV support

The core is designed to support up to the highest HDTV resolution, 1920x1080 @ 30 fps progressive. This opens a whole new range of applications from high-end video camcorders to high-resolution video surveillance at very low cost.

Low gate count

The core is designed very efficiently, with a low gate count. This allows 4CIF (704x576) video @ 30 fps to be decoded by low end FPGAs at the slowest speed grade as well as 720p (1280x720) video @ 30 fps in high end FPGAs.

Multi-channel support

The pixel processing capability of the core can be shared among multiple video channels (up to 32). Each video channel can have its own resolution and switching from one channel to the other will happen on the frame boundary. For example, at 250 MHz, up to 6 D1 (720x480) channels can be decoded simultaneously at 30 fps or up to 20 CIF (352x288) channels at 30 fps or a combination of both.

This allows for a very flexible decoding environment where multiple channels with different resolutions and frame rates are decoded by the same small core.

Progressive and interlaced video support

The core can support both progressive and interlaced video, for maximum flexibility.

No external CPU required

The core can decode video independently, without the support of an additional CPU. This represents a large cost saving compared to solutions that require an external CPU.

CBR and partial VBR supported

The core supports CBR (Constant Bit Rate). VBR (Variable Bit Rate) can only be partially supported in order to prevent the CFS from overflowing.

Performances

Performance figures of the OL_H264LD-CFS core implemented with some particular technologies are shown in the table below. All the features listed above are included in the gate count.

Technology	Approx Area	Speed	Video Throughput
0.13 μ LV 0.9V, 125 C	Data will be released soon	\sim 250 MHz	1920x1080 (1080p) @ 30 fps

Table 2 Performance of the OL_H264LD-CFS core.

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Summary

The combination of low gate count, low operating frequency, and full HDTV resolution support makes this core an application-enabling technology.

The presence of the CFS with such high compression instead of a standard external reference frame store makes this core unique for its low resource and power requirements.

This core is suitable for a wide range of applications including mobile phones, camcorders, webcams and video surveillance cameras.

Deliverables

Synthesizable VHDL or Verilog RTL.
Bit accurate C model.
Complete HDL testbench.
Complete data sheet.

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